REMARKS

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Claim Objections

Claim 1 -10 are objected to because of certain informalities. These claims have been amended to remove informalities.

Claim Rejections under 35 U.S.C. §103(a)

Claim 1, 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halim et al (US Patent 5,036,527). Applicants respectfully traverse these rejections.

There are three basic criteria to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a). First, there must be some suggestion or motivation in the cited references to modify or combine their teachings; second, there must be reasonable expectation of success; and third, the prior art references must teach or suggest all the claim limitations. *See* M.P.E.P §2142. As to claim 1, Halim et al. does not teach or suggest all the claim limitations.

First, claim 1 recites a plurality of interleaved gain and filter stages in an analog front end. In contrast, Halim et al. describes only one amplifier 12 with a plurality of predetermined discrete gain levels. Second, claim 1 recites selecting an order of gain stages where Halim et al. does not show, teach, or suggest selecting gain stages because it only contains one amplifier 12 and there is no need to select an order of gain stages. Third, claim one recites iterations of gain selection through various gain stages where Halim et al. adjusts the gain level of a single amplifier based on comparison with predetermined thresholds as identified by the first and second threshold detectors 22 and 24. Therefore, Halim et al. does not show, teach, or suggest all limitations of claim 1. Further, Halim et al. does not suggest using various interleaved gain and filter stages and the Examiner has not identified such motivation, as recited in claim 1. According to Halim et al., "[t]herefore it is an objective of the present invention to provide an apparatus and a method which allows for the accommodation of a broad dynamic range of

incoming signal levels without complicating the design or increasing the cost of an integrated circuit embodiment thereof." (Col. 6, lines 27-32, emphasis added). Accordingly, claim 1 is patentably distinguishable from Halim et al.

Claim 3 depends from claim 1 and is patentably distinguishable from Halim et al. for at least the same reasons as claim 1. Further as to claim 3, the Examiner has stated that "Halim et al teach resetting the gain counter (see column 9, line 50 - 51)." (Emphasis added). Applicants would like to respectfully point to the Examiner that in the cited sections, counters 40 and 50 are actually part of a latch counter 29 as shown in figure 2. Further, these counters are not configured to count gain stages because Halim et al. does not even have various gain stages. Halim et al. has only one gain stage with plurality of gain levels. Counters 40 and 50 contribute to the function of the latch counter 29, which according to Halim et al. "...provides both dumping and hysteresis to the comparator output signal on line 28 ..." (col. 7, lines 66-68). Halim et al. further describes the function of the latch counter 29 in col. 8, lines 1-19), which does not teach or suggest counting gain stages for various iterations as recited in claim 3. Therefore, Halim et al. does not show, teach, or suggest gain stage counter as recited in claim 3 and claim 3 is further patentably distinguishable from Halim et al.

Claim 4 depends from claim 1 and is patentably distinguishable from Halim et al. for at least the same reasons as claim 1.

Claim Rejections under 35 U.S.C. §102(b)

Claims 18 - 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Nelson et al. (US Patent 6,058,162). Applicants respectfully traverse these rejections.

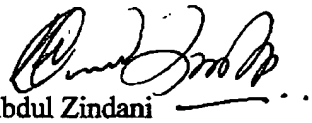
To anticipate a claim, the reference must teach each and every limitation of the claim. *See* MPEP §2131. Nelson et al. does not teach each and every limitation of claim 18. First, Nelson et al. does not show an analog front end having a plurality of serially coupled gain stages as recited in claim 18. Second, Nelson et al. does not show that the processor is adapted select a gain setting of each of said gain stages in a predetermined order as recited in claim 18 because Nelson et al. does not even show various serially coupled gain stages. Thus, the processor cannot

be adapted to select the gain stages in any order. Therefore, Nelson et al. does not teach each and every limitation of claim 18. Accordingly claim 18 is patentably distinguishable from Nelson et al.

Claims 19-20 depend from claim 1 and are patentably distinguishable from Halim et al. for at least the same reasons as claim 18.

Applicant believes this application and the claims herein to be in a condition for allowance. Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,



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